INTEGRATING INTEGRATED CIRCUIT CHIPS ON PAPER SUBSTRATES USING INKJET PRINTED ELECTRONICS

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ABSTRACT

This paper investigates the integration of silicon and paper substrates using rapid prototyping inkjet printed electronics. Various Dimatix DMP-2831 material printer settings and adhesives are investigated. The aim is to robustly and effectively connect various integrated circuit(IC) chip packages to a paper substrate using a commercially-available conductive silver ink. The verification process included contact resistance compared to line resistance, percentage effective connections, geometry relative to design parameters and frequency characteristics. These parameters are useful in solving integration difficulties and aid the development of electronic networks on paper substrates, providing a clearer understanding of rigid and flexible substrate integration.

OPSOMMING

In die huidige studie word verskeie druk verstellings van die Dimatix DMP-2831 materiaal drukker, asook aanhegtings materiale ondersoek. Die doel is om robuuste en effektiewe konneksies tussen verskeie geintegreerdestroombaanflokkie pakkies en ‘n papier substraat te bewerkstellig, deur gebruik te maak van ‘n kommersiële bekombare geleidende silwer ink. Die vergelykings parameters sluit die volgende in: kontak weerstand relatief to lyn weeerstand, persentasie effektiewe konneksies, geometrie relatief to ontwerps geometrie asook frekwensie karakteristieke. Hierdie parameters is nuttig om integrasie-probleme, weens oplyning en geleiding uitdaagings op te los. Hierdie resultate kan gebruik word in die ontwikkeling van elektroniese stroombane op papier substrate en bewerkstellig ‘n beter begrip van rigiede- en buigbaresubstraat integrasie.

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1. INTRODUCTION

Printed electronics is a fast growing field with a variety of applications, generally in the domains of flexible and low cost devices or large area display systems, such as sensors, antennas and batteries [1] - [4]. In particular, printed electronics technology promises considerable contributions to the field of low cost paper-based point-of-need diagnostics [5]. Rapid prototyping of electronic circuit designs is achievable using printable ink to form conductive tracks via digital printing technologies.

Rapid prototyping of printed electronics aids in the implementation of hybrid paper-based circuitry, namely a paper medium populated with off-the-shelf electronic chips, and can eventually lead to a fully paper-based circuit. Furthermore, printing of electronics onto paper substrates is desirable for low-cost applications, where flexibility and disposability are also requirements.

Component development using printed technologies has been successful and can act as a complimentary technology to silicon-based processes [6]. By combining commercially available components developed on the well-established integrated circuit(IC) platform with various paper-based printing techniques and components, integrated systems can be developed which take advantages from both platforms. In this way, many of the complex circuits developed for silicon do not need to be replicated on paper substrates. This paper investigates the integration of silicon-based components and paper substrates using rapid prototyping of inkjet printed electronics.

Alignment and conductivity challenges arise when combining various substrates because of their different thermal resistance levels and surface properties, thereby limiting the possible integration options [7]. Conventional screen printing has a minimum line width of 0.2 mm which results in a low resolution, whereas inkjet printing provides resolutions on paper as fine as 0.05 mm which allows for fine pitch connections [8]. Various print settings and adhesion materials were investigated to robustly and effectively connect various integrated circuit chip packages to a paper substrate. The verification process included contact resistance compared to line resistance, percentage effective connections, geometry relative to design parameters and frequency characteristics over a range of frequencies. The results showed that by printing 3 layers using 35 µm drop spacing or 1 layer using 5 µm drop spacing sufficiently connected the various integrated circuit chip packages to the paper substrate. These parameters are useful in furthering the development of electronic networks on paper substrates, and provide a clearer understanding of rigid and flexible substrate integration.

2. EXPERIMENTAL DESIGN

2.1 Design layout

Two designs were used to investigate the integration of silicon chips and paper substrates using rapid prototyping inkjet printed connections. The first design consisted of a Small Outline Integrated Circuit with 16 pins (SOIC16) as displayed in Figure 1. The second design consisted of three types of connectors for three types of commonly used silicon chip packages, namely a Small Outline Transistor (SOT23), a Small Outline Integrated Circuit with 8 pins (SOIC8) and a Light Emitting Diode (1206 LED). The design was divided into a track design, shown in Figure 2, and two types of connector designs, shown in Figure 3 and Figure 4. Two types of connector designs were required to accommodate drop spacing selection.

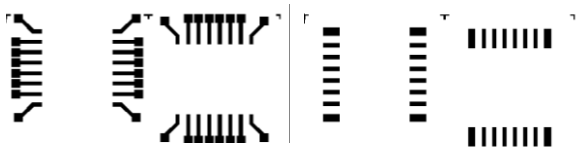


Figure 1. A layout design for the (a) tracks and (b) connections of an SOIC16 chip package.

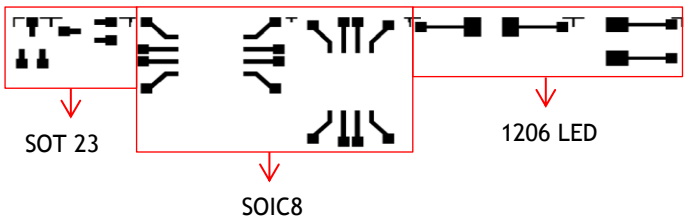


Figure 2. Track layout design.

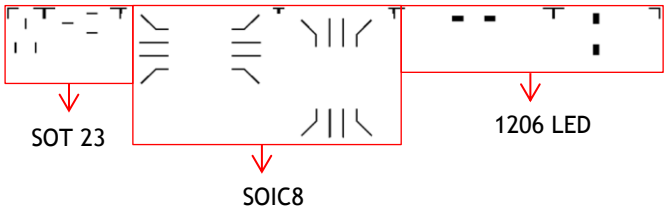


Figure 3. Connection layout design with a line width of a 100 μm.

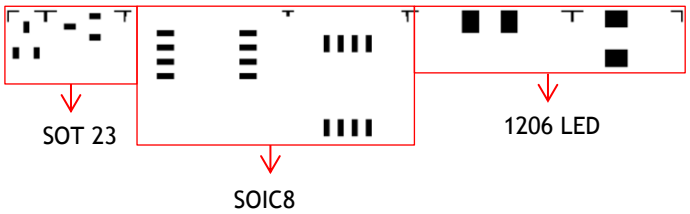


Figure 4. Connection layout design with a line width of 500 μm.

The track layout was designed according to the specific package dimensions with each pin connected to a measurement pad. The pin width of the SOT 23 and SOIC8 package is 500 μm and the 1206 LED package width is 1 mm. The 100 μm line width layout was designed for a smaller drop spacing to prevent short circuiting of pins due to excessive ink dispensed when using a smaller drop spacing [9]. Excessive ink would create a blob, thereby imitating soldering methods. A larger drop spacing leads to less ink being dispensed per design, and thus to insure contact, the contact width was increased to 500 μm to cover the whole pin [9]. For the LED package, the printed connection line width was 300 μm and 1.5 mm respectively.

2.2 Manufacturing techniques

The printed connections and tracks are printed using the Fujifilm Dimatix DMP-2831 drop-on-demand piezo inkjet printer with a mechanical resolution of 5 μm. The DMCLCP-11610 Dimatix Materials Cartridge with a minimum drop volume of 10 pl as well as 16 nozzles each having a 21

μm orifice was used. The minimum printing feature size is not only dependent on the drop volume and the orifice size, but on the drop spreading (due to the substrate properties) and drop angle [10].The Harima NPS-JL nano-paste silver conductive inkjettable ink was printed on NB-RC-3GR120 paper substrate manufactured by Mitsubishi. NPS-JL ink has a silver concentration of 56.8 wt%, a viscosity of 8.4 mPa.s and a density of 1.81 g/ml. Thermal curing was completed at either 120°C for an hour (recommended) or at 60°C for 8 hours depending on the adhesive method. The Dimatix printer settings include a jetting voltage of 33 V, a nozzle temperature of 30°C and a platen temperature of 30°C [9].

Three different commercially available adhesives were investigated in order to effectively adhere the component packages to the paper substrate. The first was precision superglue manufactured by Loctite, the second was Unplasticised Polyvinyl Chloride (PVC-U) manufactured by Tangit and the third was a general-purpose silicone adhesive manufactured by Devil.

2.3 Measurement techniques

2.3.1 Structural analysis

Laser profilometry was performed, using a confocal laser-scanning microscope (Zeiss LSM5 Pascal), for the dimensional analyses of the connections. The populated paper designs were mounted onto microscope glass slides using double-sided tape, prior to placement under the microscope for analysis.

2.3.2 Electrical track analysis

Track resistance, contact resistance and operational frequency were measured using an impedance analyzer (GW-Instek LCR-8110G). Kelvin probing was selected in order to minimize positive measurement errors generated by lead and contact resistances.

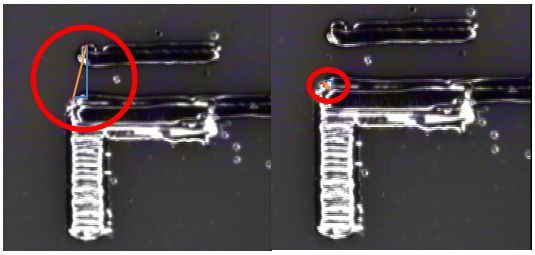
A lumped component model was used to calculate the operating frequency of the connections. However, for the resistive measurements, the measurement frequency was significantly lower than that of the cut-off frequency of the conductive connections, and thus only the resistance values were needed [10].The calculated resistance ratio of the connection resistance versus the track resistance is of importance when evaluating the quality of printed connections. This parameter indicates the quality regarding repeatability and reliability of rapid prototyping of inkjet printed electronic connections.

3. RESULTS

3.1 Alignment

The substrate was taken off of the heated printing platen before attaching the components and printing the connections. This was done in order to alleviate component detachment due to quick adhesive drying. To ensure that the tracks were properly cured, they were cured before the components were attached and the connections printed. Therefore, the alignment of the design becomes an important factor.

To ensure that the substrate was placed in the same prior position, zero-marks were hand-drawn onto the substrate. Fine alignment was achieved by using the fiducial camera of the Dimatix printer as well as the printed alignment marks, shown in Figure 5, to pin-point the exact starting position.



(a) (b)

Figure 5. Using the Fiducial camera of the Dimatix printer, (a) the offset of the misaligned printed structure is measured and (b) used to align the printed structure.

By using the fiducial camera, the alignment offset was optimised to less than 25 μm in *x- and y-axis*, well within the acceptable spacing requirement of 500 μm. The minimum printing feature size currently achievable is 50μm. If finer alignment is required thinner alignment marks must be used.

3.2 Number of effective connections

The most important attribute of a connection is to accurately connect individual parts of a system. In this analysis, 4 different drop spacing values and 3 different number of printed layers were investigated. The Dimatix printer prints in a horizontal manner and from top to bottom, therefore the attributes of horizontal and vertical connections may differ.

Figure 6 shows several SOIC16 packages connected by printing connections using 5 μm, 25 μm, 35 μm and 50 μm drop spacing for 1, 2 or 3 printed layers. Superglue was used to attach the packages to the paper after the tracks were printed prior to printing the connections. Curing was carried out at 60 °C for 8 hours.

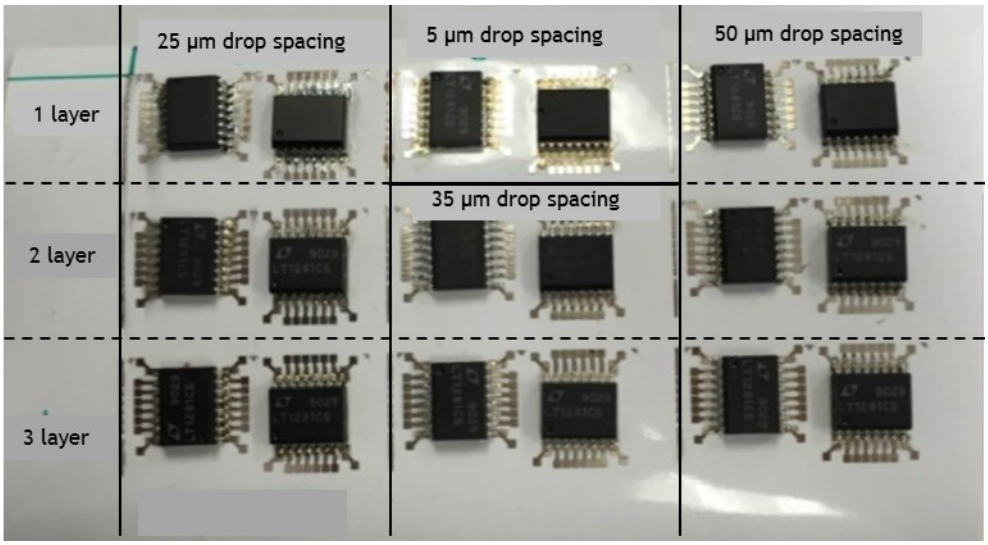


Figure 6. Connection test using a SOIC16 package.

After the manufacturing process was complete, the conductance of each pin to its related pad was measured. The number of effective connections is shown in Figure 7.

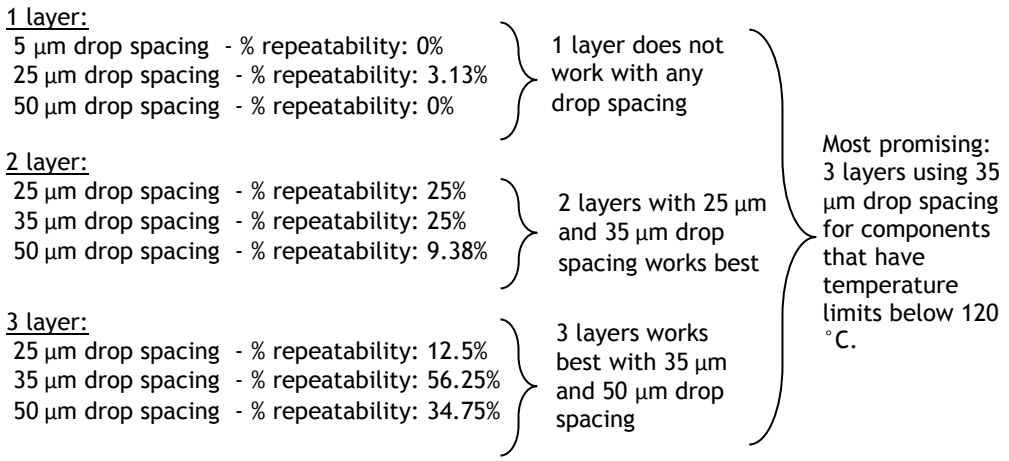


Figure 7. A diagram showing the percentage effective connections achieved when printing various layers using various drop spacing as well as which combination works best.

When using a design width of 1.5 times that of the pin width, the 5 μm drop spacing created a connection between the integrated circuit pin and the connection pad. However, it also created short circuits that rendered the circuit unusable. The 50 μm drop spacing does not create a dense enough bump to properly connect the pins to the connection pads. The 25 μm drop spacing creates open and short circuits, whereas the 35 μm drop spacing creates the fewest number of open and short circuits and creates the most effective connections below 50 Ω (which was selected as the benchmark for an effective connection).

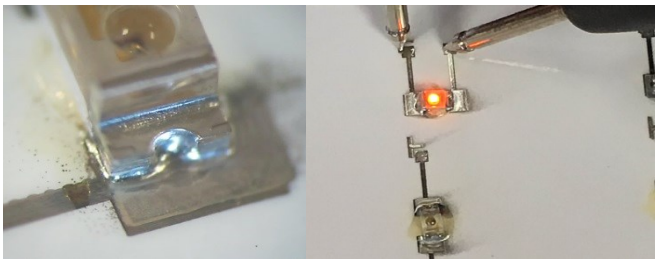
Using a 5 μm drop spacing with a normal design did not work. When reducing the design width, the excessive ink forms a blob, shown in Figure 8 (a), similar to that generated by solder, without shorting the pins. The inkjet printed pin connections, in Figure 8 (b), was printed using a 35 μm drop spacing for 3 layers, and performed the best in the previous experiment.

(a) (b)

Figure 8. Inkjet printed pin connections using (a) 5 μm drop spacing with 1 layer and (b) 35 μm drop spacing for 3 layers.

The Dimatix printer prints in a horizontal manner, therefore the number of effective connections may differ when printed vertically and horizontally. When printing with 5 μm drop spacing for 1 layer, the horizontal and vertical printing efficiency was 68.75 % and 50 %, respectively. Because of the thin lines, some of the connection tracks did not come into contact with the pins, therefore explaining the low percentage of effective connections. When printing with a 35 μm drop spacing for 3 layers the horizontal and vertical printing efficiency was 91.67 %

and 87.5 %, respectively. The LED package connection printed with a 5 μm drop spacing for 1 layer short circuited all the LEDs. Figure 9 shows the effectively connected LED packages connected using a 35 μm drop spacing.



(a) (b)

Figure 9. (a) Inkjet printed connection, connecting a (b) paper-based hybrid LED circuit.

3.3 Adhesion methods and materials

Generally when working with flexible substrates and components, the components move as the substrate moves. The same rule applies to rigid substrates and components. However, when integrating a flexible substrate with a rigid component, the flexible substrate must adhere to the rigidness of the component whilst remaining flexible. Therefore, the adhesion method and material is important. The adhesive must be both flexible and strong enough to keep the substrate connected, to the components.
Figure **10** illustrates that even though effectively connected, the components still lift off of the paper when the substrate is bent.

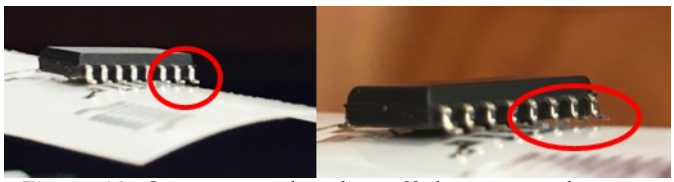
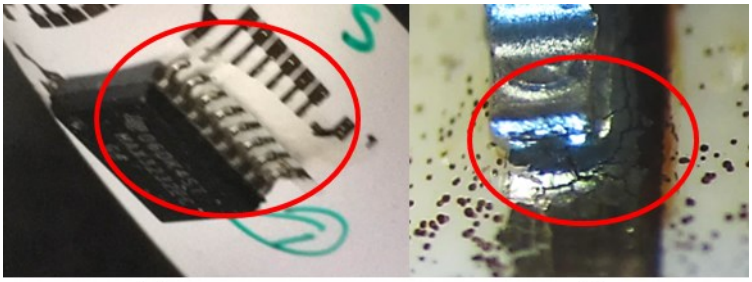


Figure 10. Components bending off the paper substrate.

In order to alleviate this problem the chip package pins were also glued to the paper so that the substrate is kept rigid around the pins but remains flexible as a unit. Although superglue is a strong adhesive, it is not flexible when dry, therefore when the paper was bent, the superglue detached from the paper and formed macro-cracks, as shown in Figure 11 (a). Furthermore, when printing on superglue the spreading of the ink changed, and caused short circuits. Micro-cracks, Figure 11 (b), were also observed after curing, which therefore disconnected the pins from the printed tracks. By adhering the pins to the paper substrate using superglue, the integration problem was transferred from the pin-track interface to the superglue-paper interface.

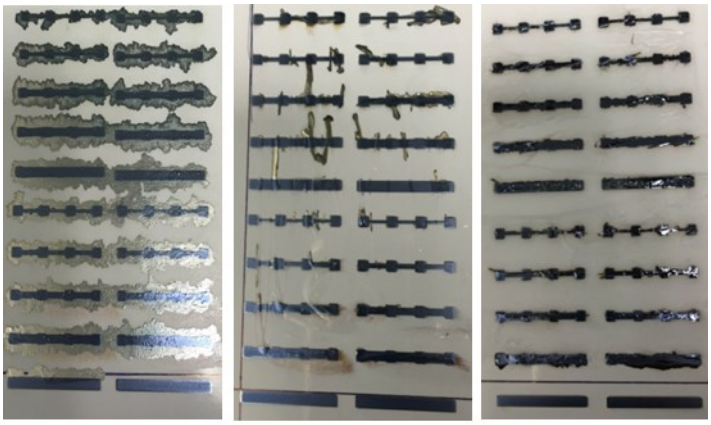


(a) (b)

Figure 11. A broken connection due to (a) a macro-crack or (b) a micro-crack.

3.3.1 House-hold adhesives

The following experiment was performed to identify common house-hold adhesives other than superglue that could be used to attach the respective media. Superglue, PVC-U and silicone adhesive was tested.



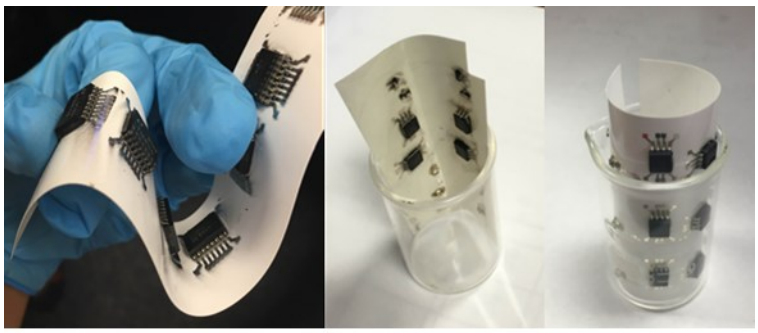
(a) (b) (c)

Figure 12. Tracks printed on (a) PVC-U cement, (b) superglue and (c) silicon adhesive.

The viability of printing tracks on other common adhesives, shown in Figure 12, was omhically tested. The silicon substrate had a high resolution and the highest flexibility, but the printed tracks were not conductive. Only the tracks on the PVC-U cement and superglue were conductive. However, the printing resolution on the PVC-U cement was too low, as shown in Figure 12 (a). The superglue substrate was the most conductive but the least flexible. From these 3 adhesives, superglue remained the best-suited when comparing household adhesives.

3.3.2 Polydimethylsiloxane (PDMS) as adhesive/coating agent

The following results show the possibility of PDMS acting as a flexible adhesive or acting in conjunction with another adhesive as a coating agent to create robust repeatable tracks. When using PDMS as an adhesive, the connections printed over the PDMS are not conductive. When using superglue as adhesive and immediately after printing the connections, coating the pins with PDMS, the connections could not cure properly and were therefore not conductive. However, when curing the tracks and connections first and then applying the PDMS, the circuit became significantly more robust and conductive, as shown in Figure 13. Three different numbers of effective connections were calculated for each setting, namely, the printed connections of the LED packages as well as the SOIC8 packages placed in a vertical and horizontal manner.



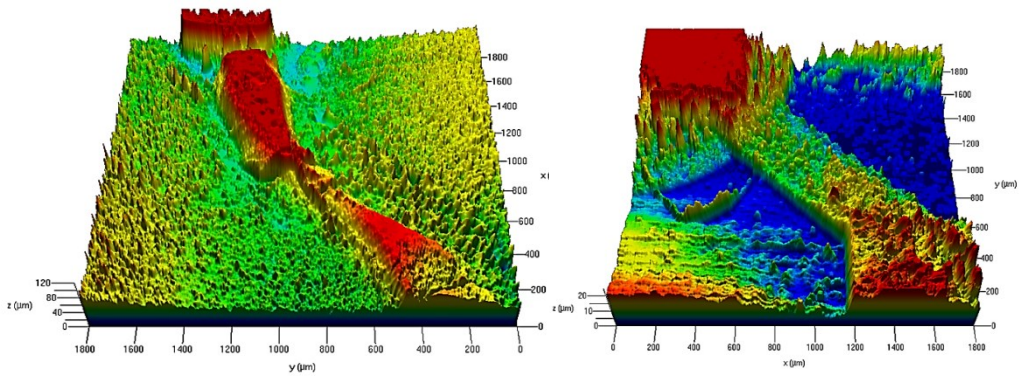
(a) (b) (c)

Figure 13. (a) A folded hybrid silicon paper-based design, (b) a horizontal inward bending test, and (c) a vertical outward bending test.

When printing with 35 μm drop spacing for 3 layers before undergoing any bending procedure, the number of effective connections were 91.67 % 83.33 % and 66.67 %. When printing with 5 μm drop spacing for 1 layer before undergoing any bending procedure the % effective connections were 0 %, 69 % and 50 %. After the bending test, which was performed around a 31 mm diameter (Figure 13 (b) and (c)), the number of effective connections of the connections printed with 35 μm drop spacing for 3 layers were 91.67%, 62.50% and 55.56% and respectively. The number of effective connections after the bending test of the connections printed with 5 μm drop spacing for 1 layer stayed the same.

3.4 Dimensional characteristics

For the dimensional characterization, laser profilometry was performed to identify the thickness of the printed connections as well as to compare the design geometry to the printed geometry. Figure 14 (a) and (b) shows the laser profilometry performed on the printed connections when using a 35 μm drop spacing for 3 layers and a 5 μm drop spacing for 1 layer, respectively.



(a) (b)

Figure 14: Laser profilometry of printed connections using (a) 5 μm drop spacing for 1 layer and (b) 35 μm drop spacing for 3 layers.

Table 1 provides the dimensional results obtained via laser profilometry.

Table 1: Geometrical results for printing with 5 µm drop spacing for 1 layer and 35 µm drop spacing for 3 layers.

Measured printing parameter[µm]	*5 µm drop spacing for 1 layer*	*35 µm drop spacing for 3 layers*
Thickness (t)	128	13.81
Width (w)	200	320

According to the designs, the printed connection width should be 100 µm and 300 µm, when either printing with a 5 µm drop spacing for 1 layer or a 35 µm drop spacing for 3 layers, respectively. When printing by using 5 µm drop spacing for 1 layer, the width is twice that of the design. However, this was expected because of the excessive ink dispersion. The thickness of the connections had a similar thickness as the pin thickness of the chip package, therefore comparable to soldering methods. When printing with a 35 µm drop spacing for 3 layers, the width had an acceptable deviation of less than 10 % from the actual design parameter.

3.5 Electrical Characterization

The electrical characterization includes the ratio of the connection resistance relative to the tracks resistance, and the frequency of operation of the connections. Figure 15 provides the results for the connection resistance relative to the track resistance of the printed connections.

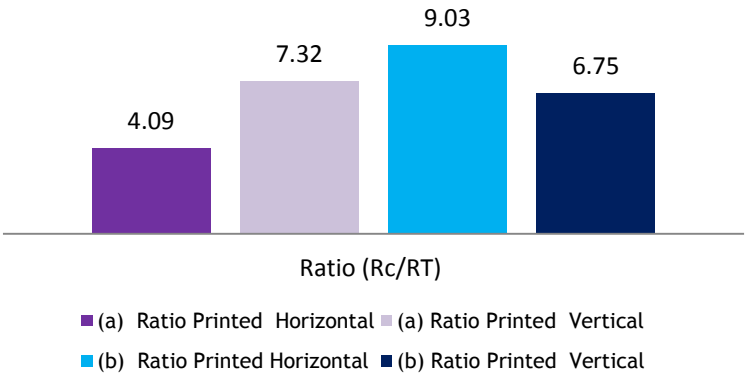


Figure 15. Electrical characterisation of the printed connections compared to similar tracks when printing with (a) a 5 µm drop spacing for 1 layer and (b) a 35 µm drop spacing for 3 layers.

In Figure 15, the track resistance is represented by R_T and the connection resistance is represented by R_C. When printing using a 5 µm drop spacing for 1 layer the ratio is lower than when printing using a 35 µm drop spacing for 3 layers. This indicates that the connections printed using a 5 µm drop spacing for 1 layer are less sensitive to the change in dimension and substrate.

3.5.1 Circuit frequency of operation

The impedance spectra for the frequency of operation for the printed connections are provided in Figure 16.

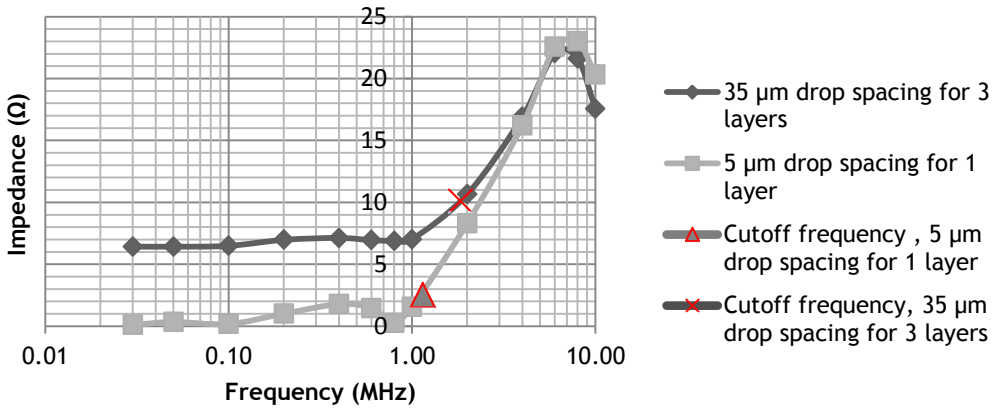


Figure 16: Bandwidth identification of connections printed with a 5 µm drop spacing for 1 layer and a 35 µm drop spacing when printing with 3 layers.

Figure 16 shows that both data lines had a similar trend that resemble a high-pass system and was therefore dominated by the series inductance present in a lumped model of a conductive track. The +3dB cut-off frequency of the connections printed with a 5 µm drop spacing for 1 layer of 1.14 MHz is lower than that of the connections printed with 35 µm drop spacing for 3 layers, which is at 1.84 MHz. The wider bandwidth of the 35 µm drop spacing indicates that its region of operation is larger. However, the impedance of the connections printed with 5 µm drop spacing for 1 layer was approximately 5 times lower than that of the connections when printing with a 35 µm drop spacing for 3 layers. This is also an important factor when considering circuit noise.

4. DISCUSSION

The results indicate that superglue as an adhesive in combination with PDMS as a coating agent creates the most robust and repeatable connections. Furthermore, after testing various printing settings, printing with a 5 µm drop spacing for 1 layer and 35 µm drop spacing for 3 layers showed the most promising results. The following key observations were made in terms of both the physical and electrical results of the mentioned printing parameters.

- When printing connections with a 35 µm drop spacing for 3 layers the number of effective connections were the highest, however after the bending test the number of effective connections decreased to a similar percentage than that observed when printing connections with a 5 µm drop spacing for 1 layer. Furthermore, after the bending test, the connections printed using a 5 µm drop spacing for 1 layer stayed the same, indicating that the connections printed using a 5 µm drop spacing for 1 layer are more robust, whilst printing with a 35 µm drop spacing for 3 layers is more repeatable.

- When connecting chip packages similar to LEDs (surface mount resistors, capacitors, etc.), printing with a 5 µm drop spacing for 1 layer dispenses too much ink, thereby short circuiting the component. Printing these connections using a 35 µm drop spacing for 3 layers is both repeatable and robust.

- The resistance and resistance ratio when printing connections with a 35 µm drop spacing for 3 layers was higher than the connections printed with a 5 µm drop spacing

for 1 layer. This indicates that when using connections printed with a 5 µm drop spacing for 1 layer the circuit noise will be lower.

- The frequency of operation of the connections when printing with a 35 µm drop spacing for 3 layers was higher than the connections printed with a 5 µm drop spacing for 1 layer, therefore providing a larger linear working range.

Table 2 summarizes the comparisons between these two printing settings.

Table 2: Summary of the better performing printing settings for various parameters.

Parameter	*Printing settings fro best performance*
Repeatability	35 µm drop spacing for 3 layers
Robustness	5 µm drop spacing for 1 layer
Compatibility with different chip packages	35 µm drop spacing for 3 layers
Resistance	5 µm drop spacing for 1 layer
Frequency of operation	35 µm drop spacing for 3 layers

These parameters can be used in making electronic circuits on paper substrates. The design parameters of this work can be further investigated and optimized by effectively connecting a bare die to a paper substrate which requires advanced alignment and fine feature sizes.

5. CONCLUSION

The integration of silicon and paper substrates by using rapidly prototyped inkjet printed connections can be created by using 35 µm drop spacing for 3 layers or 5 µm drop spacing for 1 layer in combination with superglue as an adhesive and PDMS as a coating agent. These parameters are useful in furthering the development of electronic networks on paper substrates, and provide a clearer understanding of rigid and flexible substrate integration.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

[1] Vena A., Sydanheimo L., Tentzeris M. and Ukkonen L. Vena A. 2014. "A Fully Inkjet-Printed Wireless and Chipless Sensor for CO2 and Temperature detection.," *IEEE Sensors Journal*, 99.

[2] Zheng G., Cui Y., Karabulut E., Wågberg L., Zhu H. and Hu L. 2013. "Nanostructured paper for flexible energy and electronic devices," *Materials Research Society (MRS) Bulletin*, 38(4), pp 320-325,

[3] Steckl A.J. 2013. "Circuits on cellulose," *Spectrum, IEEE*, 50(2), pp 48-61.

[4] Maxwell E.J, Mazzeo A. D. and Whitesides G. M. 2013. "Paper-based electroanalytical devices for accessible diagnostic testing," *Materials Research Science Bulletin*, 38(4), pp 309-314,

[5] Joubert T-H, Bezuidenhout P.H., Chen H., Smith S. and Land K.J. 2014. "Inkjet-printed silver tracks on different paper substrates," in *MAM'14*.

[6] PrintoCent designer's handbook, *Printed electronics and diagnostic products*, 1st ed., Antti Juusti, Markku Kylmänen and Kari Ikonen, Neficon Finland Oy Turo Piila, Ed. Kello, Finland: Neficon Finland Oy, 2015.

[7] Perelaer J., de Laat A.W.M., Hendriks C.E. and Schubert U.S. January 2008. "Inkjet-printed silver tracks: low temperature curing and thermal stability investigation," *Journal of Materials Chemistry*, 18, pp 3209-3215.

[8] Kim Y., Kim H. and Yoo H. February 2010."Electrical characterization of screen-printed circuits on the fabric," *IEEE transactions on advanced packaging*, 33(1), pp 196-204.

[9] Bezuidenhout P.H., Schoeman J. and Joubert T-H. 2016."The design and manufacturing considerations of a paper-based E. coli biosensor," in *International Conference on Competitive Manufacturing*, Stellenbosch.

[10] Bezuidenhout P.H., Smith S., Mbanjwa M., Land K.J. and Joubert T-H. 2015. "Comparison of different silver inks for printing of conductive tracks on paper substrates for rapid prototyping of electronic circuits," in *Rapid product development association of South-Africa*,