DESIGN AND IMPLEMENTATION OF A BIDIRECTIONAL CURRENT-CONTROLLED VOLTAGE-REGULATED DC-DC SWITCHED-MODE CONVERTER

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Abstract: The design and implementation of a bidirectional current-controlled voltage-regulated DC-DC converter is presented. The converter is required to connect a battery of electrochemical cells (the battery) to an asynchronous motor-drive unit via a regulated DC bus. A two-stage soft-start circuit is included to limit the peak current drawn from the battery during start-up. During normal operation the converter controls the battery current as a function of the DC bus voltage in order to regulate the DC bus. The focus of the presented work is upon the design and implementation of the current and voltage control loops, where the voltage control loop encloses the current control loop. Circuit stability is ascertained by means of both frequency and time domain analysis. It is shown that both control loops are stable and provide good transient response. The presented circuit is manufactured and tested. Test results are compared to the results of the simulation. The converter efficiency is determined by comparing the power drawn from the DC bus (with a load in place) to that drawn from the battery.

Key words: Bidirectional converter, current control, voltage control, soft-start, stability analysis.

1. INTRODUCTION

The design and implementation of a non-isolated bidirectional current-controlled voltage-regulated switched-mode DC-DC converter is presented. The converter is required to transfer up to 1 kW of electrical power between a battery of electrochemical cells (the battery) and an asynchronous motor-drive unit via a regulated DC bus. The converter is bidirectional to facilitate extended periods of regenerative braking (during which energy is returned to the battery). The bus voltage is required to be regulated in the range of 170 V to 180 V DC (175 V nominal), regardless of the direction of current flow through the battery. A relatively high bus voltage of 175 V was chosen to reduce the rated current of the circuit, thus reducing self-heating while improving the efficiency of the converter.

To facilitate the regulation of the DC bus voltage, two control loops (an inner and an outer) are employed. The inner loop measures and compares the mean battery current to a set-point current generated by the outer control loop, where the outer control loop measures and compares the DC bus voltage to a fixed set-point (corresponding to a bus voltage of 175 V DC). The current set-point, generated by the outer control loop, is limited such that the mean battery current is retained in the range of -10 A to +10 A. During start-up a two-stage soft-start circuit limits the inrush current from the battery to the DC bus.

2. BASIC CIRCUIT OPERATION

Fig. 1 outlines the plant portion of the converter circuit. While in essence a half-bridge, the circuit may be viewed as a simple boost converter with synchronous rectifier when functioning in the forward direction ($\overline{i_L}$>0), and as a simple buck converter with synchronous rectifier when functioning in the reverse direction ($\overline{i_L}$<0).

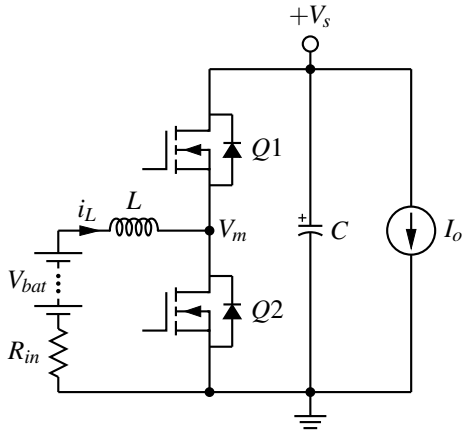

Figure 1: Bidirectional DC-DC converter circuit.

The battery comprises ten 12 V, 40 Ah rated deep-cycle lead-acid batteries. The internal battery resistance is denoted by R_{in}. MOSFET's are used as the switches and the switching frequency is set to 40 kHz. Inductor L comprises 55 turns of Litz wire of 3.8 mm^2 total cross-sectional area (120 strands of 0.2 mm diameter enamelled copper wire) wound over an Arnold A-866142-2 powdered-iron toroidal core with Al = 140 nH/turn^2, to achieve a final inductance of 420 μH.

At a mean current of 10 A the current density through the inductor windings is 2.65 A/mm^2. The value of the inductor was chosen to achieve a peak to peak current ripple of approximately 20 % of the absolute maximum value of the mean current. That is to say, 2 A.

2.1 Soft Start Circuit

The two-stage soft-start circuit comprises pre- and post-charge mechanisms [1]. The pre-charge circuit limits the peak battery in-rush current to 5 A by means of four parallel connected 100 Ω resistors. At such time as the bus capacitor C is charged to the battery potential (through the anti-parallel diode of switch Q_1) the resistors are short-circuited by a relay (effectively removing the resistors from circuit). A resistor divider (connected across the DC bus), a reference voltage source, and a comparator control the action of the relay.

The post-charge circuit continues to limit the battery in-rush current by initially setting the switching signal dead-time to maximum. This limits the on-time of the switches, thus slowing the rate at which charge is delivered to the bus (as the bus charges the remaining 120 V to 175 V), during which time the dead-time is progressively ramped down to its minimum value (where the minimum value was chosen to eliminate MOSFET shoot-through currents).

2.2 Current Limiting Circuit

An active clamp circuit [2] is used to limit the absolute maximum of the mean current demanded from the battery. This action is realised by clamping the range of the set-point current dictated by the voltage control loop.

2.3 Isolated Gate Driver Circuit

An isolated gate-drive circuit is employed to communicate the switching signals generated by the converter control circuit to the gate of each MOSFET. Galvanic isolation between the switches and the control circuit is essential to prevent damage to the control circuit (due to the large voltage excursions encountered by the MOSFET's).

Each isolated drive circuit comprises an optocoupler [3], a simple push-pull oscillator circuit (oscillating at approximately 300 kHz), a small toroidal transformer (with split primary and secondary windings), and two fast rectifier diodes. The oscillator supplies power to the output section of the optocoupler via the transformer and fast rectifier diodes, while the optocoupler communicates the switching signals.

3. PWM CONTROL CIRCUIT DESIGN

A linear model of the modulator circuit is assumed, where the duty-cycle of the PWM signal is calculated as the ratio of the error voltage V_e to the amplitude of the ramp wave V_R. The mean voltage $\overline{V_m}$ measured at the mid-point between switches $Q1$ and $Q2$, is thus the product of the duty-cycle and the mean bus voltage $\overline{V_s}$.

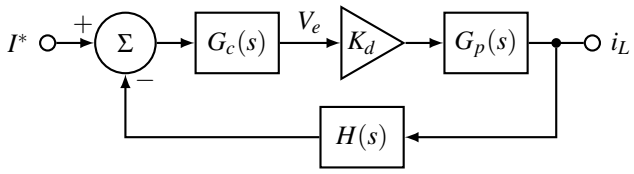

Figure 2: Current control loop.

The forward transfer function G_p describing the mean battery and inductor current $\overline{i_L}$ as a function of the duty cycle δ, is given by

$$G_p(s) = \frac{1}{sL + R_{in}}. \tag{1}$$

3.1 Current Control Loop

The current control loop, shown in Fig. 2, functions to regulate the mean inductor current flowing to and from the battery. An error voltage V_e is generated as a function of the difference between the set-point current I^* and the mean battery current $\overline{i_L}$. This error voltage is compared (by means of high-speed comparator) to a triangular waveform in order to generate the required PWM switching signals.

In the initial design of the current controller the bus voltage was assumed constant, which is reasonable given that the current control loop is designed to respond significantly faster than the voltage control loop. Once, however, the voltage and current control loops were combined, the bus voltage was considered variable.

Ten parallel connected 0.68 Ω metal film resistors were used for current sensing. The feedback voltage provided to the inverting input of the summation in Fig. 2 is thus the product of the inductor current i_L and the feedback transfer function $H(s)$, where $H(s)$ is simply the combined resistance of the current sense resistors, 0.068 Ω.

With reference to Fig. 2, the open loop transfer function is

$$G_{ol}(s) = G_c(s)K_dG_p(s)H(s), \tag{2}$$

and the closed loop transfer function is thus

$$G_{cl}(s) = \frac{G_c(s)K_dG_p(s)}{1 + G_c(s)K_dG_p(s)H(s)}. \tag{3}$$

In adherence with the Nyquist stability criterion, the open loop transfer function is required to have both positive phase and gain margin in order for the closed loop transfer function to be stable (not oscillate). The phase margin should, preferably, be at least 30° [4]. Furthermore, the unity gain crossover frequency of the open-loop transfer function should be chosen according to the desired

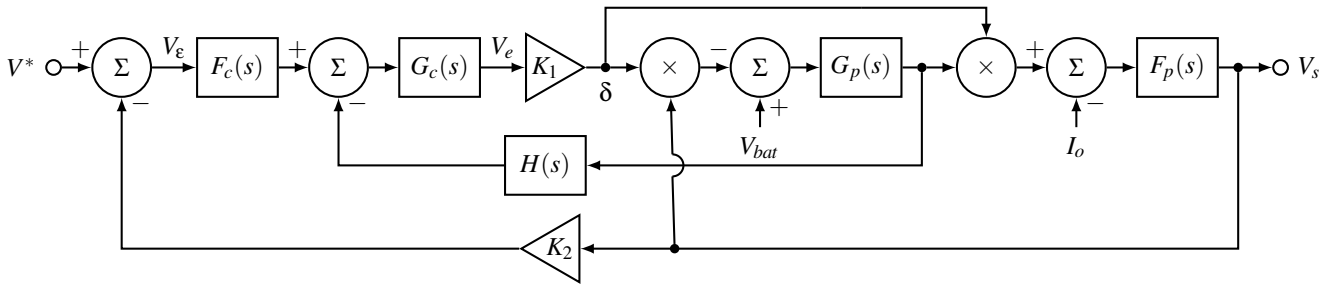

Figure 3: Voltage control loop.

performance of the system, but is generally designed to be at around one-fifth of the systems' switching frequency [5]. In accordance with the above requirements, a pole-zero compensator, also known as a type 2 amplifier, was selected as the current controller $G_c(s)$. As the name suggests, this compensator consists of a pole-zero pair, where the pole and zero are placed to achieve the required closed-loop stability of the system. This compensation method was chosen due to the good transient response and load regulation that it provides [6].

3.2 Voltage Control Loop

The combined voltage and current control loops are shown in Fig. 3. The set-point voltage V^* is indicated on the left, while the bus voltage (the object of the voltage control loop) V_s is on the right. The current control loop, described earlier, is enclosed by the voltage control loop. The bus voltage applied to the modulator circuit within the current control loop is derived from the output of the voltage control loop. The gain block K_1 represents the pulse-width modulator and outputs the switch's duty cycle δ. The bus capacitor C shown in Fig. 1, is denoted $F_p(s)$. Hence:

$$F_p(s) = \frac{1}{sC}. \tag{4}$$

Feedback provided to the inverting input of the summation on the left of the voltage control loop is a scaled version of the bus voltage, where K_2 is the scaling factor. The difference between the set-point voltage V^* and the scaled bus voltage $K_2 \times V_s$, is V_ε, which is the input to the voltage controller $F_c(s)$.

The open-loop transfer function of the voltage control loop (of which the current controller is an element) is given by

$$F_{ol}(s) = K_2 \left(\frac{(G_p(s)F_p(s)V_{bat} - 2\delta G_p(s)F_p(s)V_s}{1+\delta^2 G_p(s)F_p(s)} \right) \times \left(\frac{K_1 F_c(s)G_c(s)}{1+K_1 G_c(s)G_p(s)H(s)V_s} \right), \tag{5}$$

where

$$\delta = K_1 \left(\frac{F_c(s)G_c(s)V_\varepsilon + G_c(s)G_p(s)H(s)V_{bat}}{1+K_1 G_c(s)G_p(s)H(s)V_s} \right). \tag{6}$$

With reference to (5) and (6), it is apparent that the open-loop transfer function is non-linear. Thus, in order to undertake a Bode plot of (5), it is necessary to asume that V_s is constant, which is assuredly not the case depending upon the magnitude of the current sink or current source attached to the bus. We thus undertook multiple Bode plots of the open-loop transfer function for values of V_s in the range of 170 V to 180 V in order to ascertain stability throughout. Below or above these values we are assured that the battery current will be current-limited, where the current loop is inherently stable, regardless of the value of V_s. Furthermore, the changing bus voltage during start-up is not considered relevant for frequency domain stability analysis since the start-up voltage is controlled by the two-stage soft-start circuit. Thus, to maintain stability in the prescribed voltage range, a pole-zero compensator was also selected for $F_c(s)$. The output of $F_c(s)$ provides the current set point I^* input to the current control loop shown in Fig. 2.

3.3 Triangular Wave Generator

A 4 MHz crystal-controlled square-wave oscillator is divided down to 40 kHz using multiple D-latches, and then integrated to generate a triangular wave. The DC component is removed from the square-wave (to prevent the integration of a constant) by capacitively coupling the output of the final D-latch to the input of the integrator. The output of the integrator is buffered.

4. SIMULATION RESULTS

Frequency and time domain simulations were undertaken to ensure the stability and accuracy of the DC-DC converter design.

4.1 Frequency Domain Simulation

Bode plots of the current control open-loop and closed-loop transfer functions, (2) and (3), are shown in Fig. 4. A DC gain of 6.04 dB is indicated, corresponding to a static loop sensitivity of 2.0 A of battery current per volt of excitation applied to the set-point input. Thus, at an absolute maximum set-point voltage of 5 V, the battery current will rise to 10 A. An infinite gain margin, and a 50.6 degree phase margin are further indicated. Since an infinite gain margin cannot be realised in practice, a

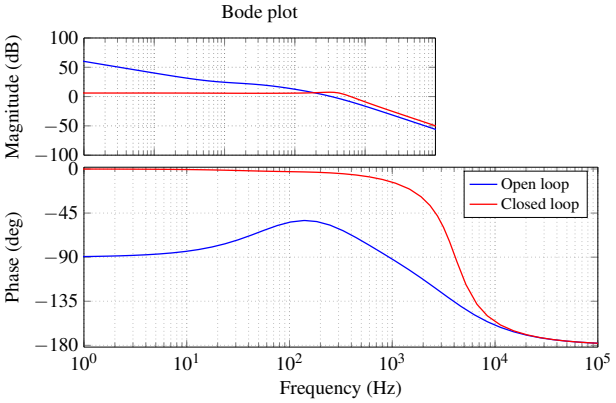

Figure 4: Current regulator bode plot.

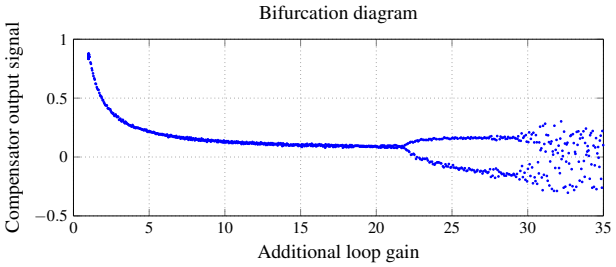

Figure 5: Bifurcation diagram used for stability analysis.

bifurcation test [7] was undertaken to determine a more realistic prediction of the gain margin. The result of the bifurcation test is shown in Fig. 5. An additional gain of 22 was added to the open-loop before the output of the compensator was observed to bifurcate, thus indicating a more realistic gain margin of 26.8 dB. Fig. 4 further indicates a unity-gain crossover frequency of 3.5 kHz, which is well below the 40 kHz switching frequency. Thus, all values within the loop may be considered to be time-averaged, as opposed to instantaneous. A positive gain and phase margin suggests that the current control loop is stable.

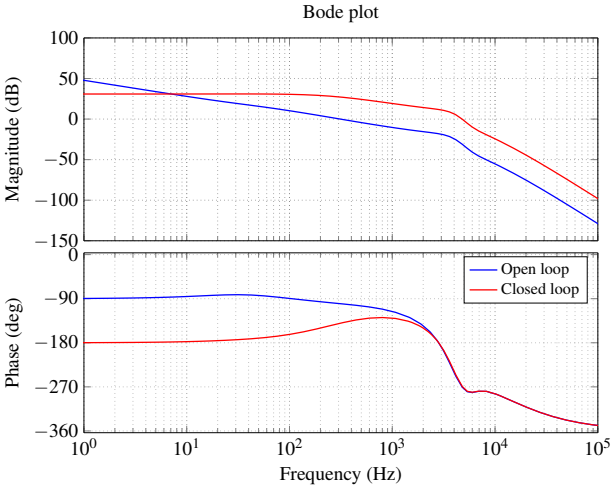

Figure 6: Voltage regulator bode plot.

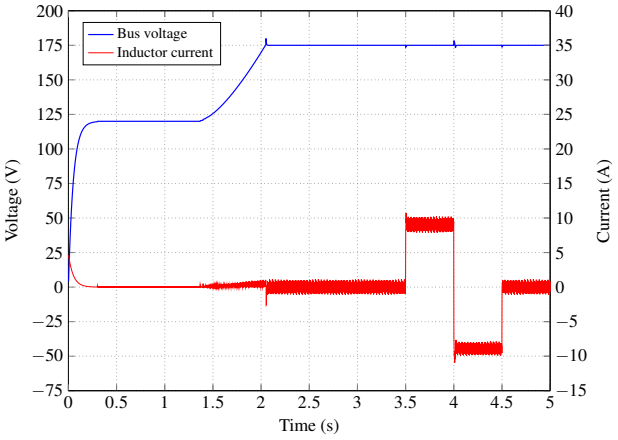

Figure 7: Time domain simulation of DC-DC converter from start-up.

Bode plots of the complete control open-loop and closed-loop transfer functions (5) and (6) at the nominal bus voltage of 175 V are shown in Fig. 6. A DC gain of 30.9 dB is indicated, corresponding to a static loop sensitivity of 35 V of bus voltage per volt of excitation applied to the set-point input. Thus, at a set-point value of 5 V, the bus voltage will rise to 175 V. A phase-margin, gain-margin and unity gain crossover frequency of 79.2 degrees, 18.1 dB and 310 Hz are further indicated, suggesting that the voltage control loop is stable.

4.2 Time Domain Simulation

To confirm the stability of the system during start-up, as well as to examine the step response of the control loop (such as when a load is applied or removed from the DC bus) a time domain simulation of the complete DC-DC converter, with current and voltage control loops, was implemented. The simulation was implemented in MATLAB^{TM} and corresponds to a simple iterative Euler solution of the relevant differential equations that describe the behaviour of the circuit. Switching and conduction losses were accounted for in the model, thus enabling a basic prediction of the converter's efficiency.

Fig. 7 shows the simulated bus voltage and battery current from the application of the battery to the converter circuit at time $t = 0$. The first stage of the soft-start circuit, the pre-charge circuit, is active for the first 200 ms after start-up, during which time the bus voltage rises from zero to the battery voltage, 120 V. At approximately 1.2 s the second stage of the soft-start circuit is activated, causing the bus voltage to rise from 120 V to 175 V over the next half-second. When the bus voltage reaches 175 V there is a small voltage overshoot of 2 V, which is within the allowed range of 170 V to 180 V. It is thus not necessary to implement any additional anti-windup scheme [8] to prevent the DC bus voltage from overshooting after reaching its nominal value of 175 V.

Fig. 7 indicates that the predicted bus voltage dips briefly to 173.9 V at 3.5 s, settling back to 175 V, when a 5.7 A

current-sink (drawing 1 kW of power) is attached to the DC bus. In response to the connected load the battery current is predicted to rise to a mean value of 9.1 A. Fig. 7 further indicates that the bus voltage peaks briefly at 178.2 V at 4.0 s, settling back to 175 V, when the 5.7 A current-sink is replaced with a 5.7 A current source (supplying 1 kW of power). This latter test was implemented to examine the bidirectional capability of the converter, in response to which the battery current was predicted to fall to a mean current of -9.1 A, indicating that the battery is being charged. At 4.5 s the current source is removed from the DC bus and the battery current observed to return to a mean value of 0 A.

In accordance with that presented above, the overall system is considered to provide good transient response at the extremes (sink or source) of its functional requirements.

Finally, the simulation predicts a current ripple of magnitude 2.2 A peak, which is approximately 20 % of absolute maximum mean current that the inductor is intended to conduct at full power (sink or source). The magnitude of the current ripple is independant of the mean current provided the bus voltage, battery voltage and inductance of the inductor remain constant. The current ripple is of saw-tooth form due to the response of the inductor to the voltage V_m at the mid-point between the two MOSFET switches, which is at either zero or bus potential depending upon the state of switches $Q1$ and $Q2$ at any given moment.

5. TEST RESULTS

The DC-DC converter and control circuit, as described above, were built and tested. Fig. 8 shows the measured DC bus voltage and time averaged battery current at start-up. We note that the magnitude and rate of change of the bus voltage is similar to the result of the time domain simulation shown in Fig. 7. The battery current is time averaged over the period of a single oscillation of the PWM oscillator in order to display the mean, as opposed to instantaneous, current.

As predicted, the bus voltage is observed to rise to the battery potential within 200 ms of connecting the battery to the converter. The bus voltage is subsequently observed to rise to and regulate at 177 V as the dead-time is progressively reduced over a period of approximately 0.5 s. We note that the bus voltage is observed to regulate 2 V higher than the nominally required value of 175 V (due to an inaccuracy in the set-point value). The battery current is observed to peak at 5 A during start-up, after which an audible click is heard as the relay short-circuits the soft-start resistors.

A 28 Ω water cooled dummy-load was employed to load the converter to approximately 1.1 kW. A converter efficiency of

$$\eta = \frac{P_{out}}{P_{in}} = 94.4\% \qquad (7)$$

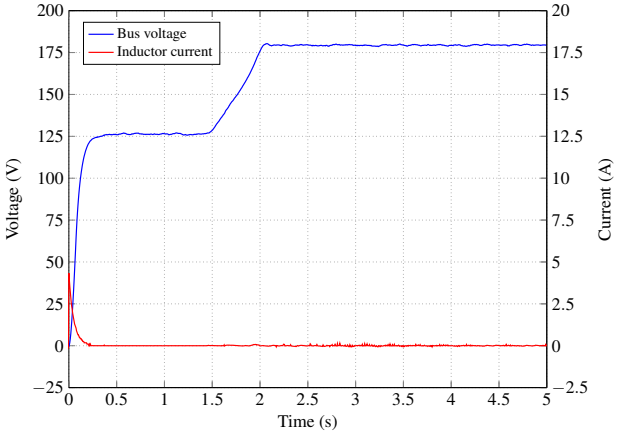

Figure 8: Experimental results: DC bus voltage and battery current during start-up.

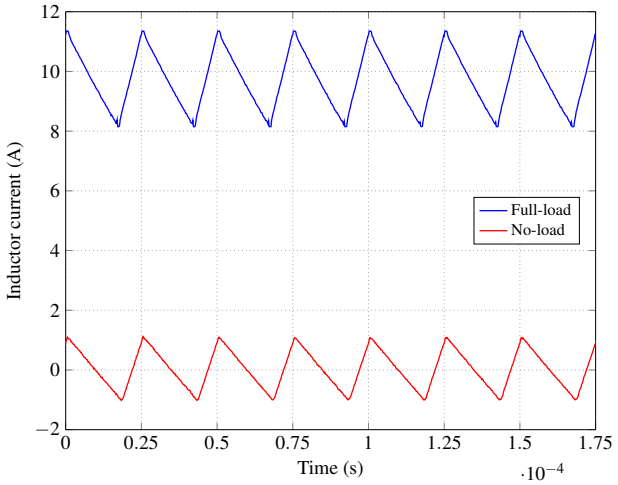

Figure 9: Experimental results: Measured inductor current.

was determined by comparing the power delivered to the load to that drawn from the battery.

The instantaneous battery current at full and zero load are shown in Fig. 9. We note that the peak to peak current increases to 3A at full load, compared to 2.2 A at zero load. This is due to a marginal decline in the inductance of the inductor, due to the decreased instantaneous permeability of the inductor core material at greater magnetisation. In both cases, the current is of saw-tooth form with a duty cycle of approximately 70 %, during which time switch Q1 is turned on and the inductor current is observed to decrease linearly.

Unfortunately, no current source (with compliance voltage as high as 175 V) was available to test the bi-directional capability of the manufactured converter. It was, however, possible to disconnect the voltage control loop in order to directly control (from an external bi-polar voltage reference source) the current control loop set-point. With the voltage regulation thus removed, a second battery of electrochemical cells (totalling 168 V) was connected to

the DC bus and the external voltage reference source employed to control both the magnitude and direction of the current between the two batteries. In this way one battery could be made to charge the other, and vice versa. A galvanometer was employed to monitor the mean current flowing to or from the 120 V battery.

6. CONCLUSION

The design and implementation of a bidirectional current-controlled voltage regulated DC-DC converter has been presented. The converter is required to interface a battery of electrochemical cells to an asynchronous motor-drive unit via a DC bus. A two-stage soft-start circuit was successfully implemented to limit the in-rush current during start-up. The converter employs both a current control and voltage control loop, where the current control loop is encircled by the voltage control loop. That is to say, the converter controls the battery current in order to regulate the bus voltage. Both control loops were shown to be stable using frequency and time domain analysis. Test results showed that the current control loop was able to regulate the mean battery current accurately. The outer voltage control loop was shown to servo the current set point in order to regulate the bus voltage to well within specification. A momentary deviation (typically lasting no more than 100 ms) from the mean of up to 2 V was observed when a 1.1 kW load was applied or removed from the bus. Simulated and test results compared well. The DC-DC converter demonstrated an efficiency of 94.4 % with the 1.1 kW load connected.

In the next stage of this project, a bidirectional asynchronous motor-drive unit will be designed and implemented in order to interface the DC bus to an asynchronous motor. The motor will ultimately sink or source power to a bi-directional mechanical load.

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