Microelectronics Journal 46(2015)310–319

A 6-bit, 500-MS/s current-steering DAC in SiGe BiCMOS technology and considerations for SFDR performance

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Abstract

This paper presents a six-bit current-steering digital-to-analogue converter (DAC), which optimises the spurious free dynamic range (SFDR) performance of high-speed binary weighted architectures by lowering current switch distortion and reducing the clock feedthrough effect. A novel current source cell is implemented that comprises heterojunction bipolar transistor current switches, negative-channel metal-oxide semiconductor (NMOS) cascode and NMOS current source to overcome distortion by specifically enhancing the SFDR for high-speed DACs. The DAC is implemented using silicon¿germanium (SiGe) BiCMOS 130 nm technology and achieves a better than 21.96 dBc SFDR across the Nyquist band for a sampling rate of 500 MS/s with a core size of 0.1 mm2 and dissipates just 4 mW compared to other BiCMOS DACs that achieve similar SFDR performance with higher output voltages, resulting in a much larger power dissipation.