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# First Principle Leakage Current Reduction Technique for CMOS Devices

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## Abstract

This paper presents a comprehensive study of leakage reduction techniques applicable to CMOS based devices. In the process, mathematical equations that model the power-performance trade-offs in CMOS logic circuits are presented. From those equations, suitable techniques for leakage reduction as pertaining to CMOS devices are deduced. Throughout this research it became evident that designing CMOS devices with high- dielectrics is a viable method for reducing leakages in cryptographic devices. To support our claim, a 22nm NMOS device was built and simulated in Athena software from Silvaco. The electrical characteristics of the fabricated device were extracted using the Atlas component of the simulator. From this research, it became evident that high- dielectric metal gate are capable of providing a reliable resistance to DPA and other form of attacks on cryptographic platforms such as smart card.The fabricated device showed a marked improvement on the I(subon)/I(suboff) ratio, where the higher ratio means that the device is suitable for low power applications. Physical models used for simulation included SI(sub3)N(sub4) and HfO(sub2) as gate dielectric with TiSix as metal gate. From the simulation result, it was shown that HfO2 was the best dielectric material when TiSix is used as the metal gate.