

Leakage Current Minimisation and Power Reduction Techniques using Sub-threshold Design

Hippolyte Djonon Tsague
Council for Scientific and Industrial Research (CSIR)
Modelling and Digital Science (MDS)
Pretoria, South Africa
hdjonontsague@csir.co.za

Bhekisipho Twala
Faculty of Engineering University of Johannesburg (UJ)
Department of Electrical and Electronic Engineering
Science Johannesburg, South Africa

Abstract

Low power IC solutions are in great demand with the rapid advancement of handheld devices, wearables, smart cards and radio frequency identification bringing a massive amount of new products to market that all have the same primary need: Powering the device as long as possible between the need to recharge the batteries while at the same time dramatically decreasing the device leakage currents. The use of sub-threshold techniques can be a powerful way to create circuits that consume dramatically less energy than those built using standard design practices. In this research, a SOI device was built to compare their electrical characteristics using Silvaco software. The comparisons were focused on three main electrical characteristics that are threshold voltage, sub-threshold voltage and leakage current. It was found that SOI devices are ideal candidates for low power operation.