Simulation and Parameter Optimization of Polysilicon Gate Biaxial Strained Silicon MOSFETs

Hippolyte Djonon Tsague
Council for Scientific and Industrial Research (CSIR)
Modelling and Digital Science (MDS)
Pretoria, South Africa
hdjonontsague@csir.co.za

Bhekisipho Twala
Faculty of Engineering University of Johannesburg (UJ)
Department of Electrical and Electronic Engineering
Science Johannesburg, South Africa

Abstract

Although cryptography constitutes a considerable part of the overall security architecture for several use cases in embedded systems, cryptographic devices are still vulnerable to the diversity types of side channel attacks. Improvement in performance of Si-MOSFETs through conventional device scaling has become more difficult, because of several physical limitations associated with the device miniaturization. Thus, much attention has recently been paid to the mobility enhancement technology through applying strain to CMOS channels. This paper reviews the characteristics of strained-Si CMOS with an emphasis on the mechanism of mobility enhancement due to strain. The device physics for improving drive current of MOSFETs is summarized from the viewpoint of electronic states of carriers in inversion layers and, in particular, the sub-band structures. In addition, design and simulation of biaxial strained silicon NMOSFET (n-channel) is done using Silvaco's Athena/Atlas simulator. From the results obtained, it became clear that biaxial strained silicon NMOS is one of the best alternatives to the current conventional MOSFET.