Scaling Ion Traps for Quantum Computing

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Abstract: The design, fabrication and preliminary testing of a chipscale, multi-zone, surface electrode ion trap is reported. The modular design and fabrication techniques used are anticipated to advance scalability of ion trap quantum computing architectures.

1. Summary

Atomic ion traps are a lead contender for implementation of quantum computing [1]. While many basic components of quantum information processing have been demonstrated in these systems, successful scaling to many qubit architectures is yet to be achieved. Here we advance toward that goal by developing a design library of components for such an architecture, which can be quickly assembled into complicated trap designs. We manufacture and test a 150 zone surface trap with six junctions, and demonstrate the first example of transport through an electrode junction on a surface electrode trap [2].

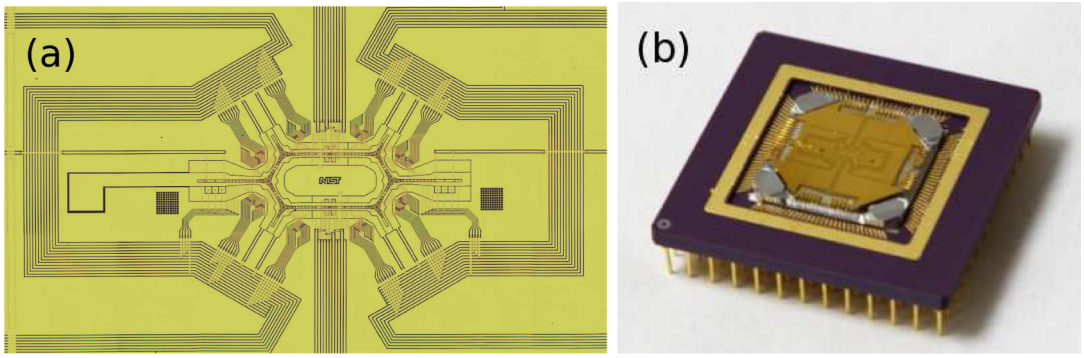

Figure 1: (a) Close-up view of multi-zone, surface electrode ion trap. (b) The trap was mounted on a 120 pin grid array.

2. References

[1] D.J. Wineland, *et al.*, Phil. Trans. R. Soc. Lond. A 361, 1349 (2003).
[2] J.M. Amini, *et al.*, New. J. Phys. 12, 033031 2010.