# A Digital Instantaneous Frequency Measurement Technique using High-Speed Analogue-to-Digital Converters and Field Programmable Gate Arrays

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***Abstract*—In modern information and sensor systems the timely estimation of the carrier frequency of received signals is of critical importance. This paper presents the Digital Instantaneous Frequency Measurement (DIFM) technique, which can measure the carrier frequency of a received waveform within a fraction of a microsecond. The resulting frequency range, resolution and accuracy of the system are scalable. The theoretical background and derivation of the technique, followed by the practical implementation of the technique on modern digital signal processing hardware will be presented. The paper concludes with functional hardware simulations as well as quantitative measurements on a prototype system.**

***Index Terms*—instantaneous frequency measurement, electronic support measures, estimation theory, digital signal processing**

## I. Introduction

The purpose of this research was to investigate the possibility of implementing a completely digital frequency estimation technique analogous to the well-known Instantaneous Frequency Measurement (IFM) technique [1] [2], which is inherently an analogue technique. It will be proven in this paper that a digital implementation of the IFM is indeed possible; yielding an all-digital estimation of the carrier frequency that is insensitive to the input signal power [3] [4]. Most importantly, it will be shown that the digital signal processing hardware requirements for a DIFM with comparable performance to the well-established analogue IFM systems are already available in the modern mid-sized Field Programmable Gate Array (FGPA).

Near instantaneous (sub-microsecond) estimation of the carrier frequency of a received waveform is of critical importance in electronic support measure subsystems (e.g. digital receiver) of an electronic warfare system [5]. A number of techniques are currently used to perform this function. The most common technique used is the all-analogue IFM technique, which will be described later. The analogue output of the IFM can be digitised and combined with basic digital signal processing to yield a Digital Frequency Discriminator (DFD). In more advanced systems, multiple IFM's are used in a single DFD to provide increased accuracy and/or bandwidth. Another technique that is regularly used in digital receiver systems is the Discrete Fourier Transform (DFT), which is typically implemented on a digital signal processor or an FPGA. The DFT is fed with a sampled and quantised replica of the input waveform generated by an Analogue-to-Digital Converter (ADC). The DFT measures the received waveforms' spectral response aliased into the 0 Hz to $f_s/2$ frequency range, where fs is the ADC sampling rate. The DFT has the important characteristic that it can estimate the spectral response of multiple time-overlapping received waveforms concurrently, whereas the IFM would yield an erroneous response in such a situation. However, the DFT has a significant disadvantage in terms of processing time, even with today's advanced FPGAs and digital signal processors. For this reason, the IFM is still the preferred frequency estimation technique employed in a number of electronic support measure systems.

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## II. Basic IFM and DFD principles

The basic principle and theory of the IFM and DFD are well documented [1] [5]. In summary, consider a given monochromatic sinusoidal input signal,

$$y(t) = A_0 \cos(2\pi f_0 t) \ , \tag{1}$$

where $A_0$ is the signal amplitude and $f_0$ is the frequency of the sinusoidal signal. This signal is split into two paths using a 3-dB coupler (Fig. 1). One of the resultant signals is delayed by a given time delay, $\tau$. The product of the signal and its delayed replica is then produced by means of an analogue diode mixer. The output signal,

$$\begin{aligned} y_{mix}(t) &= \frac{A_0^2}{4}\cos(2\pi f_0 t)\cos[2\pi f_0(t-\tau)] \\ &= \frac{A_0^2}{8}[\cos(2\pi f_0\tau) + \cos(4\pi f_0 t - 2\pi f_0\tau)] \ , \end{aligned} \tag{2}$$

consists of a constant term that is a function of the amplitude, frequency and time delay and a second harmonic term of the input frequency. If the output of the mixer is filtered with a

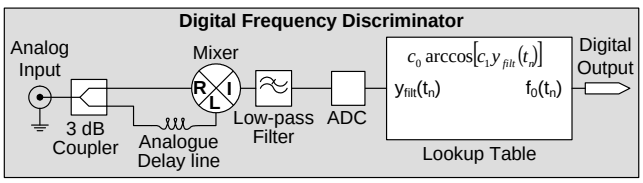


Fig. 1. Block diagrammatic description of a basic digital frequency discriminator.

low-pass filter with a cut-off frequency lower than the second harmonic, essentially only the constant term will be retained:

$$\begin{aligned} y_{filt}(t) &= \frac{A_0^2}{8}[|H(0)|\cos(2\pi f_0\tau) + |H(2f_0)| \\ &\times \cos(4\pi f_0 t - 2\pi f_0\tau + \angle H(2f_0))] \\ &\approx \frac{A_0^2}{8}|H(0)|\cos(2\pi f_0\tau) \ , \end{aligned} \tag{3}$$

where $h(t)$ and $H(f)$ are the time and frequency domain response of the low-pass filter respectively and $|H(2f_0)| << |H(0)|$. In (3), $\tau$ is chosen such that the argument of the cosine function spans the principal value range of the inverse cosine function, i.e. $2\pi f_0\tau \in [0, 2\pi]$ for all $f_0$. For a characterized filter and a fixed amplitude sinusoidal input signal, the centre frequency of the signal can be estimated as:

$$\hat{f_0} = \frac{1}{2\pi\tau}\arccos\left[\frac{8y_{filt}(t)}{A_0^2 H(0)}\right] \ . \tag{4}$$

It is common practice to sample the filter output using an ADC, yielding the sampled and quantized representation $y_{filt}(t_n)$,where $t_n = nt_s$, $n$ is the sample index and $t_s$ the sampling period of the ADC. A look-up table can then be instantiated to perform the filter output to centre frequency mapping represented in (4). It is important to realize that equations (2)-(4) are only valid for a fixed amplitude monochromatic input signal without any additive noise (amplitude or phase) and for ideal analogue components and an ideal ADC. In the presence of noise and/or multiple carriers with significant amplitude, the performance of the IFM is adversely affected. It is also greatly influenced by the non-ideal, non-linear response of the mixer and ADC especially.

## III. Calculation of the optimal time delay $\tau$

It has previously been stated that a frequency range of interest has to be chosen that has a one-to-one mapping between input frequency and output value for (3). Since

$$\lim_{f_0\to 0}[\cos(2\pi f_0\tau)] = 1 \ , \tag{5}$$

the maximum one-to-one input frequency, $f_0(max)$, can be calculated as

$$\begin{aligned} \tau &= \frac{1}{2\pi f_0(max)}\arccos(-1) \\ &= \frac{1}{2\pi f_0(max)}(1+2n)\pi \ , \ n = 0, 1, 2, \ldots \\ &= \frac{1}{2f_0(max)} \ , \ n = 0 \ . \end{aligned} \tag{6}$$

The optimum time delay is the inverse of twice the maximum input frequency. This, together with the fact that the maximum unambiguous input frequency for an ADC is half the sampling rate (also called the Nyquist rate) [6], led the authors to believe that a digital implementation of the IFM technique might prove to be an elegant solution.

## IV. Theory of the DIFM techique

### A. Basic DIFM

Suppose a DIFM is to be implemented with a frequency range equal to the information bandwidth (IBW) of a specific ADC, $IBW = f_s/2$. If the unambiguous input frequency range $[0, f_s/2)$ is chosen, the optimal time delay can be calculated from (6) as

$$\tau = \frac{1}{2\frac{f_s}{2}} = \frac{1}{f_s} = t_s \ . \tag{7}$$

Consider the sampled and quantized representation of the input signal as defined in (1):

$$\begin{aligned} y_q(n) &= Q[y(nt_s)] = Q\left[A_0\cos\left(2\pi\frac{f_0}{f_s}n\right)\right] \\ &= Q[A_0\cos(2\pi F_0 n)] \ , \ F_0 = \frac{f_0}{f_s} \\ &= \left\lfloor \frac{2A_0}{D}2^{N-1}\cos(2\pi F_0 n) + 0.5 \right\rfloor \\ &= \frac{A_0}{D}2^N\cos(2\pi F_0 n) + \epsilon_q(n) \ , \end{aligned} \tag{8}$$

where $D$ is the peak-to-peak voltage dynamic range, $N$ is the number of bits, $F_0$ is the normalized input frequency, $Q\{\ \}$ is the quantization operator and $\epsilon_q(n)$ is the quantization error. The digital equivalent of the analogue mixer output can be calculated as:

$$\begin{aligned} y_{mix}(n) &= y_q(n)y_q(n-1) \\ &= \frac{A_0^2}{D^2}2^{2N-1}[\cos(2\pi F_0) \\ &+ \cos(4\pi F_0 n - 2\pi F_0)] \\ &+ \frac{A_0}{D}2^N\{\cos(2\pi F_0 n)\epsilon_q(n-1) \\ &+ \cos[2\pi F_0(n-1)]\epsilon_q(n)\} \\ &+ \epsilon_q(n)\epsilon_q(n-1) \ , \end{aligned} \tag{9}$$

It is important to realize that the frequency component $4\pi F_0 n$, which is the $2^{nd}$ harmonic in (9), folds back in the sampled domain into the $[0, f_s/2)$ region whenever $f_0 > f_s/4$. The output of this mixing product is then processed with a digital low-pass Finite Impulse Response (FIR) filter. The FIR filter sums a series of weighted samples of the input signal to produce the output:

$$\begin{aligned} y_{filt}(n) &= \sum_{k=0}^{N} c_k y_{mix}(n-k) \\ &= \frac{A_0^2}{D^2}2^{2N-1}[|H_{LPF}(0)|\cos(2\pi F_0) \\ &+ |H_{LPF}(F_0')|\cos(2\pi F_0' n - 2\pi F_0 \\ &+ \angle H_{LPF}(F_0'))] + \epsilon_q'(n) \ . \end{aligned} \tag{10}$$

where $c_k$ are the FIR filter coefficients, $|H_{LPF}(0)|$ is the magnitude response of the FIR filter at 0 Hz, $|H_{LPF}(F_0')|$ is the magnitude response of the FIR filter at $F_0'$, $\angle H_{LPF}(F_0')$ is the phase response of the FIR filter at $F_0'$, $\epsilon_q'(n)$ is a derived error signal due to quantization and

$$F_0' = \begin{cases} 2F_0 & \text{if } f_0 \le f_s/4 \\ 1 - 2F_0 & \text{if } f_0 > f_s/4 \end{cases} \ . \tag{11}$$

Equation (11) implies that the frequency response of the DIFM is symmetrical around $f_s/4$. The output of this filter is used as the input to a look-up table that will output the estimated frequency of the input signal. The equivalent function of this look-up table can be expressed mathematically as

$$\begin{aligned} y_{out}(n) &= \frac{2^{N_{out}}-1}{2\pi} \\ &\times \arccos\left(\frac{y_{filt}(n)D^2}{A_0^2 2^{2N-1}\left|H_{LPF}(0)\right|}\right) , \end{aligned} \quad (12)$$

where $N_{out}$ is the number of bits used to represent the output word.

The advantage of this digital implementation is that the mixing product is relatively linear, which minimizes spurious responses. Furthermore, the filter response can be adapted or optimized for the specific requirements, that is, fast response versus measurement accuracy.

### *B. Amplitude-insensitive DIFM*

The DIFM as described above will exhibit the same amplitude sensitivity as would the analogue IFM. With the use of automatic gain control amplifiers and equalization filters, this can be negated to a certain degree. However, if the amplitude of the input signal to the ADC, $A_0$, could be available timeously as a digital value, a digital division operation could yield an output that is relatively insensitive to the input amplitude:

$$\begin{aligned} y_{div}(n) &= \frac{y_{filt}(n)}{A^2(n)} = \frac{y_{filt}(n)}{\left[A_0+\epsilon_a(n)\right]^2} \\ &\approx \frac{y_{filt}(n)}{A_0^2} \ , \ A_0 \gg \epsilon_a(n) \\ &= \frac{2^{2N-1}}{D^2}\left[\left|H_{LPF}(0)\right|\cos(2\pi F_0)\right. \\ &+ \left|H_{LPF}(F_0')\right|\cos\left(2\pi F_0' n - 2\pi F_0\right. \\ &+ \left.\left.\angle H_{LPF}(F_0')\right)\right] + \frac{\epsilon_q'(n)}{A_0^2} , \end{aligned} \quad (13)$$

where $A(n)$ is the digital estimation of the instantaneous amplitude and $\epsilon_a(n)$ is the error associated with this estimation. The quotient can then be used as the input to the $arccos\{\ \}$ operator, which could be implemented in numerous ways, with the most popular being a memory-based look-up table. The look-up table output, $y_{out}(n)$, finally yields an estimation of the input frequency, $F_0$, that is insensitive to the input amplitude, $A_0$.

When there is no time shift between the two multiplication operands in (9), i.e.

$$y_{mix}'(n) = y_q(n)y_q(n-0) = y_q^2(n) \ , \quad (14)$$

it is clear from (10) that the multiplication output will yield an estimate of the input amplitude if passed through the same low-pass FIR filter

$$\begin{aligned} y_{filt}'(n) &= \frac{A_0^2}{D^2}2^{2N-1}\left[\left|H_{LPF}(0)\right|\right. \\ &+ \left.\left|H_{LPF}(F_0')\right|\cos\left(2\pi F_0' n + \angle H_{LPF}(F_0')\right)\right] \\ &+ \epsilon_q''(n) \ . \end{aligned} \quad (15)$$

Substituting $A^2(n)$ in (13) with $y_{filt}'(n)$ yields the quotient

$$\begin{aligned} y_{div}(n) &= \frac{\frac{A_0^2}{D^2}2^{2N-1}a(n)+\epsilon_q'(n)}{\frac{A_0^2}{D^2}2^{2N-1}b(n)+\epsilon_q''(n)} \\ &\approx \cos(2\pi F_0) + \epsilon_q'''(n) + \frac{\left|H_{LPF}(F_0')\right|}{\left|H_{LPF}(0)\right|} \times \\ &\quad \cos\left(2\pi F_0' n - 2\pi F_0 + \angle H_{LPF}(F_0')\right) \\ &\approx \cos(2\pi F_0) \end{aligned} \quad (16)$$

if

$$\max\left\{\frac{\left|H_{LPF}(F_0')\right|}{\left|H_{LPF}(0)\right|} \ , \ \epsilon_q'''(n)\right\} \ll \cos(2\pi F_0) \ , \quad (17)$$

where

$$\begin{aligned} a(n) &= \left|H_{LPF}(0)\right|\cos(2\pi F_0) + \left|H_{LPF}(F_0')\right| \\ &\times \cos\left(2\pi F_0' n - 2\pi F_0 + \angle H_{LPF}(F_0')\right) \\ b(n) &= \left|H_{LPF}(0)\right| + \left|H_{LPF}(F_0')\right| \\ &\times \cos\left(2\pi F_0' n + \angle H_{LPF}(F_0')\right) \end{aligned} \quad (18)$$

The $arccos\{\ \}$ operator yields an estimation of the radian normalized frequency

$$y_{lt}(n) \approx 2\pi F_0 = 2\pi\frac{f_0}{f_s} \ . \quad (19)$$

The same digital architecture (hardware) yielding $y_{filt}(n)$ is therefore ideally suited to calculate $y_{filt}'(n)$. This is done by either duplicating the hardware and performing the calculation in parallel or by timesharing the same physical hardware and time multiplexing the input and output to take either a duplicate of the input as the two operands or the input and a shifted replica of the input as the two operands. The output of the hardware would then have to be demultiplexed, yielding the two filter outputs simultaneously.

One of the main advantages of the technique as described in equations (14)-(19) is that the amplitude measurement is precisely aligned with the estimation in (10). Timing is internal to the digital signal processor and no external calibration and/or alignment is required.

## V. RESULTS

An example of the amplitude-insensitive DIFM technique has been designed for implementation on a digital system comprising a 1.2 Gigasamples Per Second (GSPS) Atmel TS83102G0B ADC [7] that is connected to an Altera Stratix 1S30 FPGA [8] via two Atmel TS81102G0 demultiplexers [9], which lowers the data rate by a factor of 16 (Fig. 2). The example digital hardware can be configured as a Digital Radio Frequency Memory (DRFM) module, performing the function of a digitally controlled, active, coherent repeater.

The multiplication and FIR filter operations as described by (9), (10), (14) and (15) have been adapted for this parallelized data architecture. A $24^{th}$-order Chebychev window low-pass FIR filter was realized, yielding a cut-off frequency of 100 MHz and stop-band rejection exceeding 48 dB. This yielded a DIFM passband of 500 MHz. Furthermore, 9-bit multipliers were used for most multiplication operations, the output of

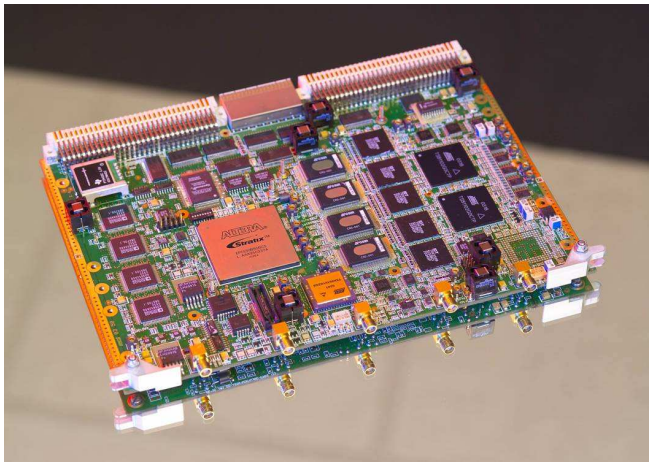

Fig. 2. DRFM hardware for implementation of DIFM.

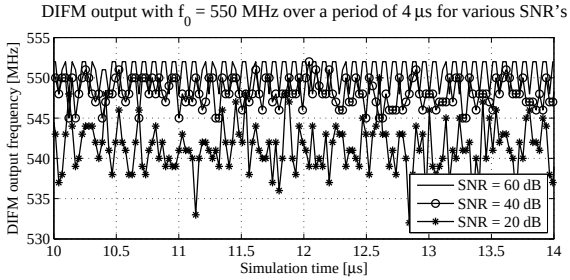


Fig. 3. Simulation results as a function of time with $f_0$ = 550 MHz for SNR $\in$ {60 dB,40 dB,20 dB}.

the FIR filters were cast as 12-bit integers, the inverse operation was implemented as a 12x12-bit look-up table with 15 dB dynamic range, and the final $arccos\{\ \}$ operation was implemented as a 12x10-bit look-up table.

The performance of this implementation was simulated in the MATLAB numerical computation environment with the main results presented below. A monochromatic input signal, having an amplitude of half of the ADC full-scale value, was injected into the DIFM and the output signal was captured for a duration of 20 $\mu$s. Coloured noise was added with a flat frequency spectrum between 50 - 550 MHz for different Signal-to-Noise Ratios (SNR's). The simulation results with $f_0$ = 550 MHz are presented in Fig. 3. With adequate SNR the DIFM output is centred on the input frequency with a maximum deviation of $\pm$2 MHz. As the SNR decreases, however, the mean output declines and the output noise increases. The main reason for this drop in the mean output is that the amplitude estimation is contaminated by the noise as the SNR decreases. The mean deviation, maximum absolute error and the Root-Mean-Squared (RMS) error are plotted as a function of frequency for the various SNRs in Fig. 4. The bias introduced for low SNR signals is obvious (Fig. 4, bottom). The maximum absolute errors and RMS errors were calculated relative to the measured mean output. At SNR levels down to 40 dB it is clear that the error is dominated by the quantization levels of the DIFM, as the error does not increase significantly. The influence of noise is clearly visible at SNR levels at and below 20 dB. The latency of this implementation

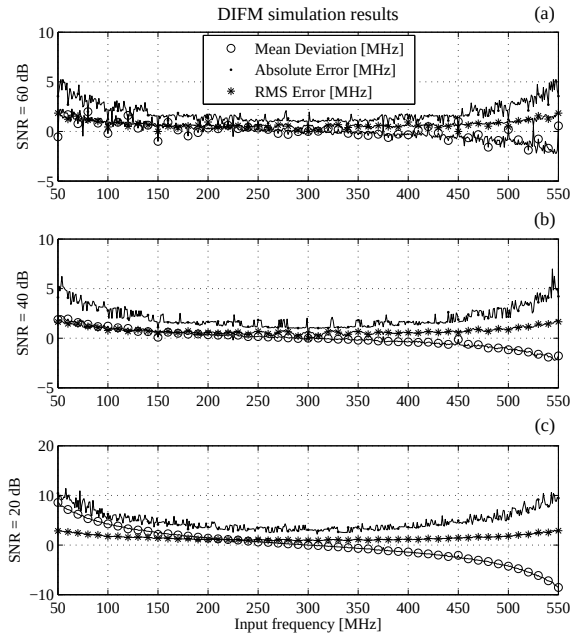


Fig. 4. Simulation results as a function of input frequency. (a) SNR = 60 dB, (b) SNR = 40 dB, (c) SNR = 20 dB.

was simulated as 13 FPGA clock cycles, which at the given clock rate yielded

$$\tau_{DIFM} = 13 \text{ cycles} \times \frac{16}{f_s} = 173.\dot{3} \text{ ns} . \quad (20)$$

The DIFM was designed to re-use the same hardware for the computation of the initial frequency estimate and the amplitude squared estimate, yielding a throughput rate of half the FPGA clock rate,

$$f_{DIFM} = \frac{f_s}{2 \times 16} = 37.5 \text{ MHz} . \quad (21)$$

Re-using the hardware realizes a smaller solution that requires less FPGA processing power. The Quartus II Ver. 5.1 firmware fitting and timing analysis software [10] predicted a maximum clock speed in excess of 75 MHz and FPGA resource usage of less than 10 % for the 1S30 device. This bodes well for the implementation of the DIFM in parallel to the DRFM control firmware on the FPGA in the example implementation hardware depicted in Fig. 2. The major advantage of having this parallel frequency estimation is that the estimate is exactly aligned with the DRFM data and no external alignment is required. Furthermore, there is no need for additional analog down-conversion or signal conditioning hardware.

The minimum pulse width yielding a stable output was simulated as 48 ADC samples,

$$T_{DIFM} = \frac{48}{f_s} = 40 \text{ ns} . \quad (22)$$

The illustrative implementation was conducted on a custom built hardware module and the results were verified by visual inspection by sweeping the input frequency and power from 50 MHz to 550 MHz and 0 dBm to -15 dBm, respectively. The

TABLE I
PERFORMANCE COMPARISON WITH OPERATIONAL SYSTEMS.

| Performance indicator | L-Band system | S-Band sytem | C-Band system | X-Band system | Ku-Band system | DIFM |
|---|---|---|---|---|---|---|
| Bandwidth (MHz) | 1060 | 2120 | 4240 | 4240 | 6360 | 500 |
| Resolution (MHz) | 0.52 | 1.04 | 2.08 | 2.08 | 3.12 | 1 |
| RMS accuracy (MHz) | 1.25 | 2.5 | 5.0 | 6.5 | 12.0 | $<2$ |
| Latency (ns) | 185 | 150 | 135 | 135 | 130 | 173 |
| Minimum pulsewidth (ns) | 95 | 60 | 45 | 45 | 40 | 40 |
| Dynamic range (dB) | 70 | 70 | 70 | 65 | N/A | 15 |

simulated results are compared to that of operational systems [5] in Table I. It is important to note that operational systems obtain the high dynamic range performance by first detecting the signal amplitude and then setting the gain of the front-end receiver to yield fixed input amplitude to the IFM. The DIFM has an instantaneous dynamic range of 15 dB that is limited by the dynamic range of the digital inversion operator and can be enhanced by increasing the number of bits used during the inversion operation or by using a more complex inversion operation. Furthermore, the DIFM bandwidth is limited by the clock rate of the ADC and the order of the FIR filter, with the relationship being approximately

$$BW_{DIFM} = \frac{f_s}{2.4} \ . \tag{23}$$

The DIFM performance can be increased significantly at the expense of using more FPGA processing resources. For example, latency can be improved by adopting a fully-parallel solution that requires almost double the resources, resolution can be increased by expanding the width of the final look-up table and accuracy can be improved by increasing the width of the multipliers and inverse operator or by raising the order of the low-pass filters.

## VI. CONCLUSIONS

We have shown that the DIFM is a viable frequency estimation technique that can be implemented efficiently in current commercial hardware, yielding results comparable to existing analogue techniques. The main shortcoming of the example implementation is the instantaneous bandwidth obtainable. With the rapid increase in ADC clock rates, however, this might even improve DIFM bandwidth performance beyond that of current operational systems. Single ADC clock rates exceeding 2.5 GSPS and time-interleaved ADC clock rates of up to 10 GSPS have been reported [11] [12] that would yield a DIFM with an approximate bandwidth of 4.16 GHz.

One of the key features of the DIFM technique, however, is its flexibility and ability to be optimized for specific requirements. It is also possible to change its characteristics in real-time by changing the filter coefficients on-the-fly. The biasing effect at low SNR levels can be reduced by designing the FIR filters to have lower cut-off frequencies. The adverse effect of doing this would be increased latency, once again highlighting the importance of performing a proper requirement analysis and trade-off study before designing a DIFM.

The DIFM is insensitive to temperature and does not require periodic calibration to maintain its accuracy. These characteristics make the DIFM operationally superior to its analogue counterparts [13].

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